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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/742,236	12/22/2000	Yoshihiko Suemura	043034/0163	7174

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EXAMINER	
HENNING, MATTHEW T	
ART UNIT	**PAPER NUMBER**
2131	

DATE MAILED: 09/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/742,236	SUEMURA, YOSHIHIKO	
	Examiner	Art Unit	
	Matthew T. Henning	2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This action is in response to the communication filed on 7/11/2005.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/11/2005 has been entered.

Response to Arguments

Applicant's arguments with respect to claims 1-19 have been considered but are moot in view of the new ground(s) of rejection.

All rejections and objections not specifically presented below have been withdrawn.

Claims 1-19 have been examined.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laughlin (U.S. Patent Number 5,553,175), further in view of Manchester et al. ("IP Over SONET")

hereinafter referred to as Manchester; and further in view of Bright et al. (US Patent Number 5,694,473) hereinafter referred to as Bright.

Regarding claim 1, Laughlin disclosed a switch having input ports and output ports, said switch operative for switchably interconnecting said input ports with said output ports (See Laughlin Fig. 20 and Col. 14 Paragraphs 3-4); a plurality of input interfaces each connected to a corresponding input port of the switch (See Laughlin Fig. 20 Elements 286), wherein each of the input interfaces inputs data to sequentially output to the corresponding input port of the switch. (See Lauglin Col. 14 Paragraphs 3-4); and a plurality of output interfaces each connected to a corresponding output port of the switch (See Laughlin Fig. 20 Elements 290), wherein each of the output interfaces inputs frames from the corresponding output port of the switch to output frames of original data (See Laughlin Col. 14 Paragraphs 3-4), but failed to disclose scramblers at the inputs and descramblers at the outputs. However, Laughlin did disclose the switch being utilized in a Synchronous Optical NETwork (SONET) (See Laughlin Col. 3 Lines 20-23).

Manchester disclosed that in order to send IP data over a SONET, the bits being transmitted should be randomized and Manchester recommended that the pseudo-random Self-Synchronizing Scrambler at the optical transmitter and the corresponding Descrambler at the optical receiver, used in ATM on SONET, should be used for this purpose (See Manchester Page 139 Col. 1 Paragraph 4 and Figure 4). Manchester further disclosed that this scrambler is reset at startup (See Manchester Page 139 Col. 2 Paragraph 1). Manchester further disclosed that upon startup or reframe the first 43 bits of data would be lost during synchronization (See Manchester Page 139 Col. 2 Paragraph 1).

It would have been obvious to the ordinary person skilled in the art at the time of invention to employ the teachings of Manchester to the optical switch of Laughlin by placing the self-synchronizing scramblers of Manchester at the inputs of the switch and by placing the self-synchronizing descrambles at the outputs of the switch. This would have been obvious because the ordinary person skilled in the art would have been motivated to provide a randomized bit stream to the optical fiber in order to thwart malicious attacks directed towards controlling the transition density of the line and to ensure that line rate recovery was possible at the receiver. Furthermore, in this combination, because the scramblers are all connected to the inputs of the same switch, it would have been obvious that they all simultaneously reset at the startup of the switch. It would also have been obvious that the descramblers be simultaneously reset after a propagation delay of the data through the switch. This would have been obvious due to the nature of the descrambler being initialized by the scrambled data input to the descrambler.

Bright teaches that in order to solve the loss of data while a self synchronizing descrambler synchronizes with the scrambler, when a scrambler and descramble begin communicating, initialization data should be sent from the scrambler to the descrambler prior to the message data in order to synchronize without losing any message data (See Bright Col. 1 Lines 47-67, and Fig. 1). Bright further teaches that the initialization data should be used to initialize both the transmitting device and the receiving device (See Bright Col. 5 Paragraph 2).

It would have been obvious to the ordinary person skilled in the art at the time of invention to employ the teachings of Bright in the combination of Laughlin and Manchester by sending initialization data to both the scramblers and descramblers when they began communicating with each other. This would have been obvious because the ordinary person

skilled in the art would have been motivated to prevent the loss of 43 bits of data during synchronization. It would have been obvious in this combination that the scramblers and descramblers would begin communicating with each other at reset and further upon switching. As such, synchronization would have be maintained after switching.

Regarding claim 11, the combination of Laughlin, Manchester, and Bright disclosed a scramble control method for a switching system, said switching system comprising: a switch having input ports and output ports, said switch operative for switchably interconnecting said input ports with said output ports (See Laughlin Fig. 20 and Col. 14 Paragraphs 3-4); a plurality of input interfaces each connected to a corresponding input port of the switch (See Laughlin Fig. 20 Elements 286), each of the input interfaces including a scrambler, each scrambler having a pseudo-random pattern generator (See the rejection of claim 1 above and Manchester Fig. 4), wherein each of the input interfaces inputs data to sequentially output frames including scrambled data (See the rejection of claim 1 above and Bright Fig. 1) to the corresponding input port of the switch (See Lauglin Col. 14 Paragraphs 3-4); and a plurality of output interfaces each connected to a corresponding output port of the switch (See Laughlin Fig. 20 Elements 290), each of the output interfaces including a descrambler, each descrambler having a pseudo-random pattern generator (See the rejection of claim 1 above and Manchester Fig. 4), wherein each of the output interfaces inputs frames including scrambled data (See the rejection of claim 1 above and Bright Fig. 1) from the corresponding output port of the switch to output frames of original data (See Laughlin Col. 14 Paragraphs 3-4), said scramble control method comprising the steps of: at each of the scramblers, generating a scrambler state indicating a value of a pseudo-random pattern generated by the pseudorandom pattern generator of the scrambler in frame timing (See

the rejection of claim 1 above and Bright Fig. 1 and Col. 5 paragraph 2); assembling a frame including the scrambler state (See Bright Fig. 1); and transferring the frame including the scrambler state to the switch (See the rejection of claim 1 above and Bright Col. 5 Paragraph 2); and at each of the descramblers, receiving a frame including a scrambler state that is the scrambler state of a corresponding scrambler that assembled the frame (See the rejection of claim 1 above and Bright Col. 5 Paragraph 2); and resetting the pseudorandom pattern generator of the descrambler to initialize the pseudorandom pattern generator of the descrambler with the value of the pseudorandom pattern indicated by the scrambler state, wherein the descrambler can be synchronized with the corresponding scrambler after the switch performs a switching operation (See the rejection of claim 1 above and Bright Col. 5 Paragraph 2).

Regarding claim 16, the combination of Laughlin, Manchester, and Bright disclosed a switching system comprising: a switch having input ports and output ports, said switch operative for switchably interconnecting said input ports with said output ports (See Laughlin Fig. 20 and Col. 14 Paragraphs 3-4); a plurality of input interfaces each connected to a corresponding input port of the switch (See Laughlin Fig. 20 Elements 286), each of the input interfaces including a scrambler, each scrambler having a pseudo-random pattern generator (See the rejection of claim 1 above and Manchester Fig. 4), wherein each of the input interfaces inputs data to sequentially output frames including scrambled data (See the rejection of claim 1 above and Bright Fig. 1) to the corresponding input port of the switch (See Lauglin Col. 14 Paragraphs 3-4); and a plurality of output interfaces each connected to a corresponding output port of the switch (See Laughlin Fig. 20 Elements 290), each of the output interfaces including a descrambler, each descrambler having a pseudo-random pattern generator (See the rejection of claim 1 above and Manchester

Fig. 4), wherein each of the output interfaces inputs frames including scrambled data (See the rejection of claim 1 above and Bright Fig. 1) from the corresponding output port of the switch to output frames of original data (See Laughlin Col. 14 Paragraphs 3-4), a reset pulse generator for generating a scrambler reset pulse and a descrambler reset pulse, wherein the scrambler reset pulse is sent to all the scramblers at equal timing, and the descrambler reset pulse is sent to all the descramblers at equal timing (See Manchester Page 139 Col. 1 Paragraph 7 – Col. 2 Paragraph 1. Further see Laughlin Col. 14 Lines 47-51); wherein each of the pseudorandom pattern generators of the scramblers and descramblers generates the same pseudorandom pattern when initialized with a same input value (See the rejection of claim 1 above and Manchester Page 139 Col. 1 Paragraph 4); wherein the pseudorandom pattern generators of the scramblers are initialized to the same input value when the scramblers receive the scrambler reset pulse so as to synchronize the scramblers (See the rejection of claim 1 above and Bright Col. 5 Paragraph 2); wherein the pseudorandom pattern generators of the descramblers are initialized to the same input value when the descramblers receive the descrambler reset pulse, so as to synchronize the descramblers and to establish synchronization between the scramblers and the descramblers (See the rejection of claim 1 above and Bright Col. 5 Paragraph 2); and wherein synchronization between the scramblers and the descramblers is maintained after the switch performs a switching operation (See the rejection of claim 1 above).

Regarding claim 18, the combination of Laughlin, Manchester, and Bright disclosed a switching system comprising: a switch having input ports and output ports, said switch operative for switchably interconnecting said input ports with said output ports (See Laughlin Fig. 20 and Col. 14 Paragraphs 3-4); a plurality of input interfaces each connected to a corresponding input

port of the switch (See Laughlin Fig. 20 Elements 286), each of the input interfaces including a scrambler, each scrambler having a pseudo-random pattern generator (See the rejection of claim 1 above and Manchester Fig. 4), wherein each of the input interfaces inputs data to sequentially output frames including scrambled data (See the rejection of claim 1 above and Bright Fig. 1) to the corresponding input port of the switch (See Lauglin Col. 14 Paragraphs 3-4); and a plurality of output interfaces each connected to a corresponding output port of the switch (See Laughlin Fig. 20 Elements 290), each of the output interfaces including a descrambler, each descrambler having a pseudo-random pattern generator (See the rejection of claim 1 above and Manchester Fig. 4), wherein each of the output interfaces inputs frames including scrambled data (See the rejection of claim 1 above and Bright Fig. 1) from the corresponding output port of the switch to output frames of original data (See Laughlin Col. 14 Paragraphs 3-4), a scramble state generator for determining a scrambler state indicating a value of a pseudorandom pattern generated by the scramble state generator, at predetermined intervals (See the rejection of claim 1 above and Bright Col. 3 Paragraph 3 and Col. 5 Paragraph 2); wherein each of the pseudorandom pattern generators of the scramblers and descramblers generates the same pseudorandom pattern when initialized with a same input value (See the rejection of claim 1 above and Manchester Page 139 Col. 1 Paragraph 4); wherein the scrambler state is sent to the scramblers, and the scramblers are simultaneously reset to the value of the pseudorandom pattern indicated by the scrambler state, so as to synchronize the scramblers (See the rejection of claim 1 above and Bright Col. 5 Paragraph 2); and wherein the scrambler state is sent to the descramblers with a delay of time period required for transferring a frame from an input interface to an appropriate output interface through the switch, and the descramblers are simultaneously reset to the value of the

pseudorandom pattern indicated by the scrambler state, so as to synchronize the descramblers and to establish synchronization between the scramblers and descramblers (See the rejection of claim 1 above and Bright Col. 5 Paragraph 2); wherein synchronization between the scramblers and the descramblers is maintained after the switch performs switching (See the rejection of claim 1 above).

Regarding claim 19, the combination of Laughlin, Manchester, and Bright disclosed a switching system comprising: a switch having input ports and output ports, said switch operative for switchably interconnecting said input ports with said output ports (See Laughlin Fig. 20 and Col. 14 Paragraphs 3-4); a plurality of input interfaces each connected to a corresponding input port of the switch (See Laughlin Fig. 20 Elements 286), each of the input interfaces including a scrambler, each scrambler having a pseudo-random pattern generator (See the rejection of claim 1 above and Manchester Fig. 4), wherein each of the input interfaces inputs data to sequentially output frames including scrambled data (See the rejection of claim 1 above and Bright Fig. 1) to the corresponding input port of the switch (See Lauglin Col. 14 Paragraphs 3-4); and a plurality of output interfaces each connected to a corresponding output port of the switch (See Laughlin Fig. 20 Elements 290), each of the output interfaces including a descrambler, each descrambler having a pseudo-random pattern generator (See the rejection of claim 1 above and Manchester Fig. 4), wherein each of the output interfaces inputs frames including scrambled data (See the rejection of claim 1 above and Bright Fig. 1) from the corresponding output port of the switch to output frames of original data (See Laughlin Col. 14 Paragraphs 3-4), wherein each of the scramblers further comprises: a scramble state generator for determining a scramble state indicating a value of a pseudorandom pattern generated by the pseudorandom pattern generator

of the scrambler in frame timing (See the rejection of claim 1 above and Bright Col. 3 Paragraph 3 and Col. 5 Paragraph 2); and an assembler for assembling a frame including the scrambler state (See Bright Fig. 1 and Col. 3 Line 60 – Col. 4 Line 2); and each of the descramblers further comprises: a reset circuit for resetting the pseudorandom pattern generator of the descrambler to a value of a pseudorandom pattern indicated by a received scrambler state included in a received frame that is received from the switch, said received scrambler state being the scrambler state of a corresponding scrambler that assembled the received frame (See the rejection of claim 1 above and Bright Col. 5 Paragraph 2); wherein the descrambler can be synchronized with the corresponding scrambler after the switch performs a switching operation (See the rejection of claim 1 above).

Regarding claims 2 and 17, the combination of Laughlin, Manchester and Bright disclosed that the scramblers and the descramblers operate according to a predetermined system clock (it was inherent that the scramblers and descramblers operated according to a predetermined system clock in order for the shift registers of Manchester Figure 4 to operate as required by the scramblers), wherein the scramblers are simultaneously initialized at a first time point and thereafter are not reset (See Manchester Page 139 Col. 2 Paragraph 1), and the descramblers are simultaneously initialized at a second time point and thereafter are not reset, wherein the second time point is delayed from the first time point by a time period required for transferring a frame from an input interface to an appropriate output interface through the switch. It was inherent that the descramblers were initialized at a point in time after the initialization of the scramblers because the descramblers are initialized by the output of the scramblers, which is

received through the switch after a propagation delay (See Manchester Page 139 Col. 2 Paragraph 1).

Regarding claim 3, the combination of Laughlin, Manchester and Bright disclosed that the first time point is a time when the switching system starts up (See Manchester Page 139 Col. 2 Paragraph 1).

Regarding claims 4 and 13, the combination of Laughlin, Manchester and Bright disclosed that the scramblers and descramblers are of frame synchronizing type (See the rejection of claim 1 above and Bright Fig. 1 and Col. 5 Paragraph 2).

Regarding claims 5 and 14, the combination of Laughlin, Manchester and Bright disclosed that a cycle of the pseudorandom patterns generated by the pseudorandom pattern generators of the scramblers and descramblers is set to be longer than a length of the frame (See Manchester Page 139 Col. 1 Paragraph 7 – Col. 2 Paragraph 1 and Bright Col. 4 Paragraph 5).

Regarding claims 6 and 15, the combination of Laughlin, Manchester and Bright disclosed that the pseudorandom pattern generators of the scramblers and descramblers use a generator polynomial specified by: $1 + X^{43}$ (See Manchester Page 139 Col. 1 Paragraph 4 and Figure 4).

Regarding claim 7, the combination of Laughlin, Manchester and Bright disclosed a scramble state generator for determining a scrambler state indicating a value of a pseudorandom pattern generated by the scramble state generator, at predetermined intervals (See the rejection of claim 1 above and Bright Col. 3 Paragraph 3 and Col. 5 Paragraph 2); sending scrambler state to the scramblers so that the scramblers are simultaneously reset to the value of the pseudorandom pattern indicated by the scrambler state (See the rejection of claim 1 above and Bright Col. 5

Paragraph 2); and sending the scrambler state to the descramblers with a delay of time period required for transferring a frame from an input interface to an appropriate output interface through the switch so that the descramblers are simultaneously reset to the value of the pseudorandom pattern indicated by the scrambler state (See the rejection of claim 1 above and Bright Col. 5 Paragraph 2)

Claim 8 is rejected for the same reasons as claim 4 above.

Claim 9 is rejected for the same reasons as claim 5 above.

Claim 10 is rejected for the same reasons as claim 6 above.

Regarding claim 12, the combination of Laughlin, Manchester and Bright disclosed that the scramblers are of self-synchronizing type (See Manchester Page 149 Col. 1 Page 4).

Conclusion

Claims 1-19 have been rejected.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Rose (US Patent Number 6,909,785) disclosed a synchronization method for use in a self synchronizing cipher.

b. Lang (US Patent Number 5,835,602) disclosed a self synchronous scrambler.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew T. Henning whose telephone number is (571) 272-3790. The examiner can normally be reached on M-F 8-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on (571) 272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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